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Specification and Drawings, as originally filed, with Application for Patent Serial No: **2,332,705**, on January 26, 2001, by **CATENA TECHNOLOGIES CANADA, INC.**, assignee of Andreas Weirich and Allan Isfan, for "A System and Method for Overlaying a DSL Access Multiplexer Onto Existing Access Systems by Reusing Test Buses".

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ABSTRACT

A digital subscriber line access multiplexer overlay onto a digital loop carrier system for transporting high speed digital data over an existing backplane which carries voice, data, and test signals, between voice line cards and a carrier line, the voice signals being time division multiplexed (TDM) into frames, the system comprising: a data bus interface for impressing the high speed data on a subset of existing backplane buses for transport along the backplane and for retrieving high speed digital data from the backplane buses; and a plurality of data line cards for connecting to the backplane and backplane subset conductors, the data line cards being adapted to couple the high speed data between the subscriber line and the backplane, whereby the high speed digital data can be routed over the backplane subset to any of the digital data line cards without interfering with the voice signals routed to voice line cards.

A System and Method for Overlaying DSL Access Multiplexer (DSLAM) onto Existing Access Systems by using Test Buses

The present invention relates generally to the field of Digital Subscriber Lines (DSLs), and particularly to a system and method for implementing DSL technology at remote access terminals.

BACKGROUND OF THE INVENTION

In order to relieve the shortage of copper subscriber lines from a telephone central office to a telephone subscriber residence, and also to reduce the length of such lines, access concentrators are frequently employed. Access concentrators employing a digital multiplex carrier to carry many individual voice conversations on a single, or several, multiplex carriers are known as Digital Loop Carriers (DLCs).

Figure 1 illustrates a block diagram of typical DLC represented generally by the numeral 10. A number of individual twisted pair subscriber lines 12 are terminated by line cards 14. In the case of typical residential telephone service, the lines 12 are terminated by POTS line cards 14, which provides a number of functions required to operate a telephone or other terminal 16 connected to the line 12 at the subscriber's residence. These functions usually include, but are not limited to:

- Battery - supplying power to the subscriber terminal;
- Overvoltage - protecting the line card against environmentally caused overvoltages;
- Ringing - supplying a ringing signal;
- Supervision - detecting when a subscriber lifts the telephone receiver;
- Coding - converting the analog line signal into digital representation;
- Hybrid - separating the received from the transmitted signals; and
- Termination - terminating the line with a required standard electrical impedance.

These functions are often collectively referred to as BORSCHT.

Each line card produces a signal in a format suitable for being multiplexed with other line card signals onto a common Time Division Multiplexed (TDM) bus 18 although other buses may be employed. Typically, each line signal is sampled at an

8kHz rate and each sample converted into a digital codeword, each usually consisting of 8 bits using one of several standard coding formats known as □□law PCM or A law PCM. The resulting bit rate per terminated line is, therefore, 64kb/s.

The codewords from one terminated line 12 or line card 14 are interleaved with those of other lines 12 and line cards 14, onto the TDM bus 18. The codewords are then commonly transmitted over a backplane to a common element, herein called a Transmit and Receive Unit/ Line Interface Unit (TRU/LIU) 20 by assigning one or several timeslots to each line card. The TRU/LIU performs two main functions:

1. electrically driving and receiving signals to/from the TDM Bus 18, clock generation, timeslot control, and the like; and
2. interface to a Digital Multiplex Carrier 21, by means of a Digital Carrier Interface 22 , which possibly includes but is not limited to line coding, line quality monitoring, clock recovery, synchronization, loopbacks, framing, alarm detection, multiplexing of signaling bits, maintenance channel termination, maintenance and remote monitoring functions. Common digital multiplex line interfaces include electrical (T1, E1) and optical (OC3, OC12) interfaces.

In order to allow for the electrical testing of subscriber lines 12 and line cards 14, a Test Access Unit (TAU) 30 is typically provided. The TAU is connected to all line cards 14 in the DLC by means of a Test Bus 32. Test buses implementations and characteristics vary widely depending on the particular embodiment and design of the DLC. Typically, in a DLC designed and intended primarily for multiplexing voice services, the Test Bus characteristics are intended to be electrically suitable for voice signals, but not necessarily for high speed digital signals, such as digital logic or DSL signals.

The TAU is typically controlled by a Control Unit 40, which may communicate with the TAU and other units in the DLC by means of a Control Bus 41.

Figure 2 illustrates the TAU and Line Card in greater detail. Here a plurality of Line Cards 14 and a TAU 30 are interconnected for line and circuit testing purposes by a Test Bus 32.

A Test Bus 32 typically groups a number of independent conductors together into one or more logical buses. Without loss of generality , the Test Bus 32 in Figure 2 has been shown to be logically grouped into 4 subsets herein labeled, with no intended loss of generality, TestOut2, TestIn2, TestOut4, and TestIn4. This illustrates two relevant concepts: 1) some line cards communicate with a subscriber terminal using 4 or more wires and may consequently require 4-wire test buses; 2) capability to simultaneously test the subscriber line (known as the test out function) and the Line Interface Circuit 18 of the Line Card 14 (known as the test in function) may be provided by means of distinct subsets of the Test Bus.

Figure 2 also shows the constituent functional blocks of a 2-wire Line Card 14. The TDM and Control Interface (TCI) 13 contains circuitry to electrically interface to the TDM Bus 18 and the Control Bus 41, as well as provide general control functions for the Line Card. The Line Interface Circuit (LIC) 11 provides the BORSCHT functions described above. The Test Relay 15 provides a means for electrically isolating the LIC from the Subscriber Line 12, connecting the LIC to the TestIn2 bus, and connecting the Subscriber Line 12 to the TestOut2 Bus.

Operation of 4-wire line cards (not shown) is a logical extension of the above with respect to test relay connectivity with corresponding 4-wire test buses.

Figure 2 also shows constituent functional blocks of the Test Access Unit 32. The Terminations block 34 contains a plurality of electrical terminations required in order to enable meaningful electrical tests of the Line Interface Circuit 11 or the Subscriber Line 12 to be performed via the Test Bus. The Switch Matrix 33 provides appropriate means, typically relays or other electrically controllable switches, to electrically connect one or more subsets of the Test Bus to one or more of a set of line terminations in the Terminations block and/or to the external Test Pair 31, either individually, jointly, or severally. A Control Interface 32 contains circuitry to electrically interface with the control Bus 41, provide general control functions, provide specific control functions to actuate the appropriate relays (or other interconnection devices) in the Switch Matrix 33. The Control Interface may also function to relay communications to and from the Control Unit (by means of the Control Bus) to and from an external device connected by means of a Control Interface Port 35. An example of such an external device might be a

keyboard and display enabling a craftsperson to control the testing of lines of line cards by means of keyboard commands.

Both the Test Relay 15 and the Switch Matrix 33 are responsive to the Control Unit 40, which in turn may be responsive to commands from a Test Controller (not shown).

In many instances, it is desirable to upgrade an existing DLC to enable the provision of new services, specifically for Digital Subscriber Line (DSL) services, and especially ADSL. Since the bit rate per subscriber line for such a service is many times that for which a voice DLC was engineered, and requires the processing of data protocols, such an upgrade becomes problematic.

In order to provide DSL service to a subscriber already served by a voice-only DLC requires changes to hardware. This change may necessitate the physical reconnection of a subscriber's line to a completely different DSL-capable DLC, if one is available at the site. If a DSL-capable DLC is not available, one may need to be installed to serve that subscriber, if space is available in the remote cabinet. If there is insufficient unused space in the cabinet or there is another reason why a new DLC cannot be installed, the subscriber may be denied DSL service altogether.

It is an object of the present invention to obviate or mitigate some of the above disadvantages.

SUMMARY OF THE INVENTION

In accordance with this invention there is provided a data bus interface for impressing the high speed data on a subset of existing backplane buses for transport along the backplane and for retrieving high speed digital data from the backplane buses, wherein, the existing backplane carries voice, data, and test signals, between voice line cards and a carrier line.

In one aspect the voice signals are time division multiplexed (TDM) into frames.

In accordance with another aspect of the invention there is provided a plurality of data line cards for connecting to the backplane and backplane subset conductors, the data line cards being adapted to couple the high speed data between the subscriber line and the

backplane, whereby the high speed digital data can be routed over the backplane subset to any of the digital data line cards without interfering with the voice signals routed to voice line cards.

BRIEF DESCRIPTION OF THE DRAWINGS

A better understanding of the invention will be obtained by reference to the detailed description below in conjunction with the following drawings in which:

Figure 1 is a block diagram of a typical Digital Loop Carrier according to the prior art;

Figure 2 is a schematic diagram of a TAU and line card of figure 1;

Figure 3 is a block diagram of a Digital Loop Carrier with overlaid DSL Access Multiplexer according to an embodiment of the present invention; and

Figure 4 is a schematic diagram showing an their interconnection of an Enhanced Test Access Unit and an Enhanced Line Card with a subset of the Test Bus.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

For convenience, like structures in the drawings are referred to using like numerals.

Figure 3 shows the architecture of the DSLAM overlay on an existing DLC 10 represented generally by the numeral 30. An Enhanced Test Access Unit 50 and DSL Enhanced Line Card 60 provide DSL service to DSL Modems 61 while maintaining POTS service to existing lines 12 and voiceband subscriber terminals 16.

Key to the operation of the DSLAM overlay, and the novel application central to this invention, is

1) the reuse of a subset of the Test Bus, hereinafter called and shown in Figure 2 as the Data Bus 70, for the transport of data streams to and from the DSL Enhanced Line Cards 60, in lieu of its previous function of the carriage of test signals; and
2) the combining of functionality of the Test Access Unit with a data aggregation and multiplexing function.

Without intending a loss of generality, Figure 2 illustrates the use of the Test Bus subsets TestOut4 and TestIn4 as the Data Bus for the transport of the data bit streams. The previous functions of the TestOut4 and TestIn4 buses is, in general, no longer available when used as a Data Bus, and may consequently result in the loss of some line and line

card testing capabilities. For example, and with no loss of generality intended, the use of the TestOut4 and TestIn4 buses might result in the loss of testing capability for 4-wire interfaces, but not of testing capability for 2-wire interfaces. The provision of adequate data bit rates for the aggregation and multiplexing of data streams from a plurality of DSL Enhanced Line Cards requires the Data Bus to carry signals of a significantly higher bandwidth than the voiceband test signals previously carried. There exist a wide variety of DLC system implementations for which the above described overlayment is possible, including, but not limited to, SLC Series 5 Carrier System, SLC-2000 Access System, SLC Series 96 Carrier System.. Details of implementation, such as number of test buses conductors, their arrangement, the assignment of these conductors to various testing and test access functions, and their electrical characteristics may differ from system type to system type. Significant engineering challenges may need to be overcome to ensure adequate transmit and receive signal integrity of, and appropriate bus access protocols for these data streams on the existing physical transmission media of the DLC, since the test buses are generally not intended or dimensioned for such purposes. The bus access protocols are likely to require solution of design issues with respect to new line card discovery and registration with the aggregation controller, addressing, transmission request and contention resolution, priority determination, synchronization, framing, fair access of multiple line cards to a single shared bus, ATM cell queuing and buffering with multiple Qualities of Service, and others. These protocols are the subject of other patent disclosures.

Figure 4 illustrates the Enhanced Test Access Unit 50, the Enhanced Line Card 14, and their interconnection by means of a subset of the Test Bus in greater detail.

The Enhanced Test Access Unit 50 expands the functionality of the previously described TAU 30 by adding the following functions: a Master Data Bus Interface (MDBI) 36; a Cell Aggregation Multiplexer (CAM) 37; a Digital Carrier Interface (DCI) 38; and a Control Processor 39. The CAM, DCI, and Control Processor are well known in the art and need not be discussed here in detail.

The MDBI is the master element in the transmission, reception, and protocol implementation for the Data Bus. The MDBI contains all the functions required to communicate over the Data Bus 70 with the DBI 61. It provides clocking, framing, cell

address translation, data recovery, cell queuing, and other functions required for the appropriate operation of the Data Bus. The MDBI and DBI together embody nad implement the Data Bus access protocols and design considerations previously described. The MDBI also provides a suitable interface to effect data or cell transfer to the CAM.

The CAM receives and transmits data to and from the MDBI. This data may exist in the format of ATM (Asynchronous Transfer Mode) cells, Ethernet packets, or other data packets or formats which are contained in the combined data streams from a plurality of DSL enhanced line cards. Without limiting the generality of the discussion, the descriptions that follow will refer to ATM cell handling only. The CAM buffers cells in queues, alter cell headers, controls the sequence of the outflow of cells as required to provide a ATM multiplexing, cell flow control, Quality of Service management, policing, shaping, etc. suitable to an ATM access Multiplexer function as is well known in the art. The CAM 37 then forwards the cells/packets on to a data network through the Digital Carrier Interface (DCI) 38.

The DSL Line Card 34 expands the functionality of the previously described Line Card 14 by adding the following functions: a Data Bus Interface (DBI) 61, a DSL Termination Unit-Central (DTU-C) 62, and a Broadband Line Interface 63. Certain types of DSL signals, such as Asymmetric DSL (ADSL) conforming to ITU G.922 standards, may coexist on a single line with POTS analog signals. It is, therefore, desirable to provide a line card capable of simultaneously communicating DSL and POTS signals between the subscriber line 12 and the DLC backplane buses.

The DBI 61 consists of all functions required to communicate over the Data Bus 70 with the MDBI 36 of the ETAU 50. These may include, but are not limited to, Data Bus protocol implementation, clock recovery and synchronization circuitry, electrical drivers, receivers, and timing circuits. The DBI implements the necessary circuitry to conform to the Data Bus protocol requirements of fair access of multiple line cards to a single shared bus, ATM cell queuing and buffering with multiple Qualities of Service, and others. The DBI is used for impressing a digital signal at a high onto the existing conductors of the backplane Data Bus, and for providing elastic stores to match the burst transmission characteristics of the Data Bus to the continuous bit stream transmitted and received from the DTU-C 62.

The DTU-C (also referred to as a data pump) consists of all circuitry normally required to convert a bit stream to/from signals which can be transmitted on a twisted pair subscriber line according to standard or proprietary protocols and modulation algorithms including, but not limited to, CAP, G.lite, ANSI T1.413. Such devices are well known in the art and do not need to be described in detail.

The Broadband Line Interface performs all the functions of a Line Interface Circuit 11 for both POTS signals as well as for the DSL signals transmitted and received by the DTU-C. The Broadband Line Interface may include separate POTS Line Interface, DSL Line Interface, and POTS Splitter, or may implemented as unified circuitry not requiring a POTS Splitter. Such devices are well known in the art and do not need to be described in detail.

Although the invention has been described with reference to certain specific embodiments, various modifications thereof will be apparent to those skilled in the art without departing from the spirit and scope of the invention as outlined in the claims appended hereto.

THE EMBODIMENTS OF THE INVENTION IN WHICH AN EXCLUSIVE PROPERTY OR PRIVILEGE IS CLAIMED ARE DEFINED AS FOLLOWS:

1. A digital loop carrier overlay system wherein high speed digital data is transported over a subset of a preexisting backplane test bus generally not intended to carry high speed digital data, and which backplane also carries voice signals, between voice line cards and a digital carrier line, the voice signals being time division multiplexed (TDM) into frames, the system comprising:

(a) a plurality of data line cards for connecting to said subset of backplane test bus, said data line cards being adapted to couple said high speed data between the backplane and a subscriber line; and

(b) an enhanced test access unit for impressing said high speed data onto a subset of the preexisting test bus for transport along said backplane and for retrieving high speed digital data from said subset of the preexisting test bus, whereby said high speed digital data can be routed over said backplane to any of said digital data line cards without interfering with the voice data routed to voice line cards.

2. A system as defined in claim 1, said data line card being an xDSL line card.

3. A system as defined in claim 1, said data line card comprising:

(a) an xDSL termination unit for converting a signal on said loop to a high speed bitstream; and

(b) a test bus subset interface circuit for impressing said high speed bitstream onto a subset of the preexisting test bus for transport along said backplane to said enhanced test access unit and for retrieving high speed digital data from said subset of the preexisting test bus for coupling to said xDSL termination unit.

4. A system as defined in claim 1, said data line card being a combined POTS and xDSL line card, said combined POTS and xDSL card including:

(a) an xDSL termination unit for converting a signal on said loop to a high speed bitstream; and

(b) a test bus subset interface circuit for impressing said high speed bitstream onto a subset of the preexisting test bus for transport along said backplane to said enhanced test access unit simultaneous with transmitting POTS signals to preexisting TDM bus for transport to preexisting transmit and receive unit, and for retrieving high speed bitstream data from said subset of the preexisting test bus simultaneous with retrieving POTS signals from said preexisting TDM bus, and coupling to said combined POTS and xDSL broadband line interface.

5. An enhanced test access unit for digital loop carrier transmission systems comprising:
   (a) means for impressing high speed data onto a subset of the preexisting test bus for transport along said backplane and for retrieving high speed digital data from said subset of the preexisting test bus, whereby said high speed digital data can be routed over said backplane to any of said digital data line cards without interfering with the voice data routed to voice line cards.
   (b) means for aggregating and multiplexing the high speed data from a plurality of data line cards in accordance with established methods and criteria well known in the art for such aggregation functions
   (c) means for interfacing and transmitting aggregated bitstreams to a digital carrier for transmittal to a data network.

6. An enhanced test access unit as in claim 5 for a SLC Series 5 Carrier System.

7. An enhanced test access unit for digital loop carrier transmission systems as in claim 5, said enhanced test access unit also including:
   (a) means for effecting test access to any or all of , test terminations, and test control with functions and interfaces substantially identical to those of the preexisting test access unit of the relevant preexisting digital loop carrier system.

8. An enhanced test access unit as in claim 7 for a SLC Series 5 Carrier System.

9. A data line card for digital loop carrier transmission systems wherein high speed digital data is transported over a subset of a preexisting backplane test bus generally not intended to carry high speed digital data, and which backplane also carries voice signals, between voice line cards and a digital carrier line, the voice signals being time division multiplexed (TDM) into frames, comprising:
   (a) means for impressing high speed data onto a subset of the preexisting test bus for transport along said backplane and for retrieving high speed digital data from said subset of the preexisting test bus, whereby said high speed digital data can be routed over said backplane to any of said digital data line cards without interfering with the voice data routed to voice line cards.
   (b) an xDSL termination unit for converting a signal on said loop to a high speed bitstream

10. A data line card as in claim 9 for a SLC Series 5 Carrier System.

11. A data line card as in claim 9, said line card being a combined POTS and xDSL line card, said combined POTS and xDSL card including:
   (a) an xDSL termination unit for converting a signal on said loop to a high speed bitstream; and
   (b) a test bus subset interface circuit for impressing said high speed bitstream onto a subset of the preexisting test bus for transport along said backplane to said enhanced test access unit simultaneous with transmitting POTS signals to preexisting TDM bus for transport to preexisting transmit and receive unit, and for retrieving high speed bitstream data from said subset of the preexisting test bus simultaneous with retrieving POTS signals from said preexisting TDM bus, and coupling to said combined POTS and xDSL broadband line interface.

12. A combined POTS and xDSL line card as in claim 11 for a SLC Series 5 Carrier System.

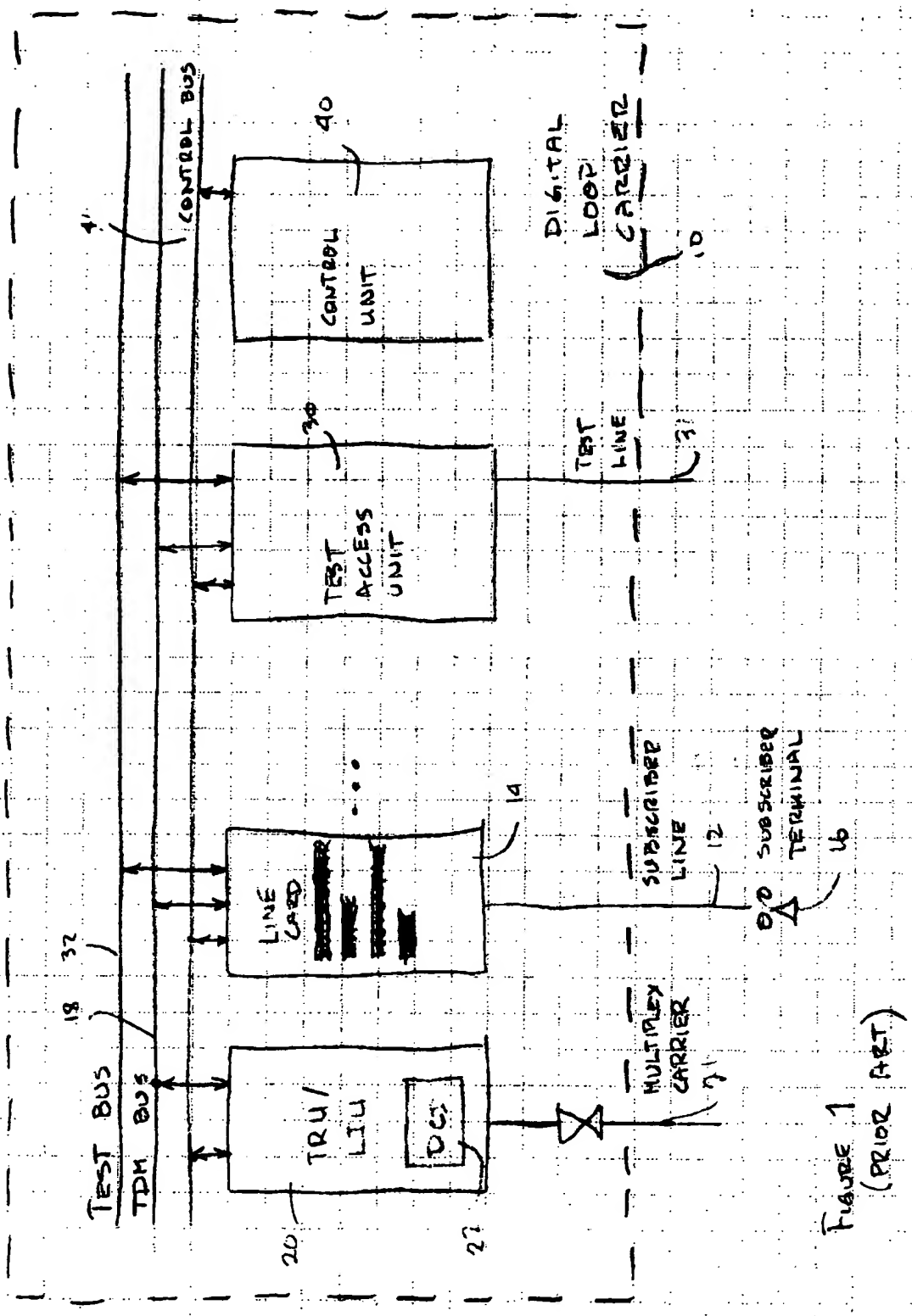

FIGURE 1
(PRIOR ART)

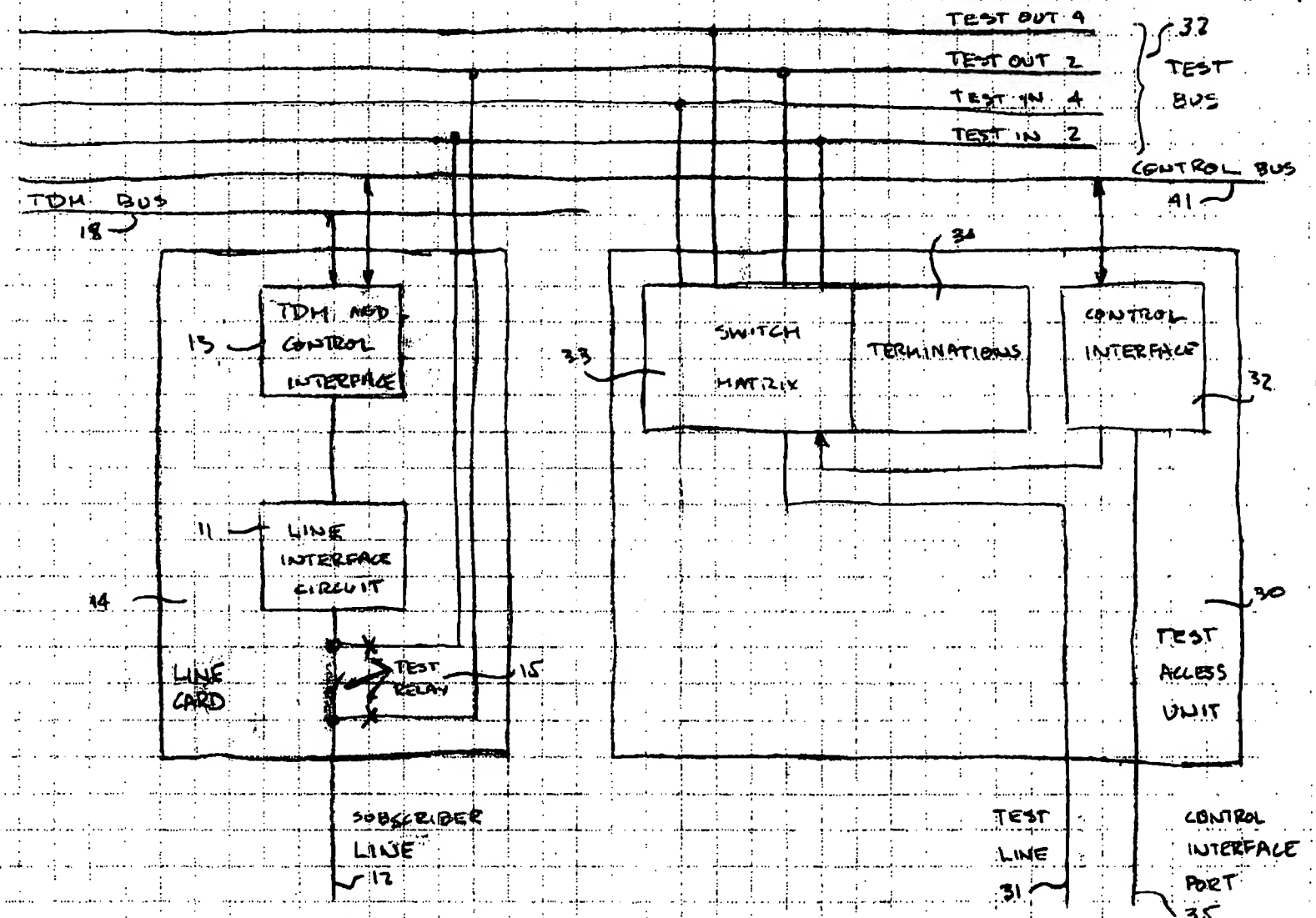

FIGURE 2
(PRIOR ART)

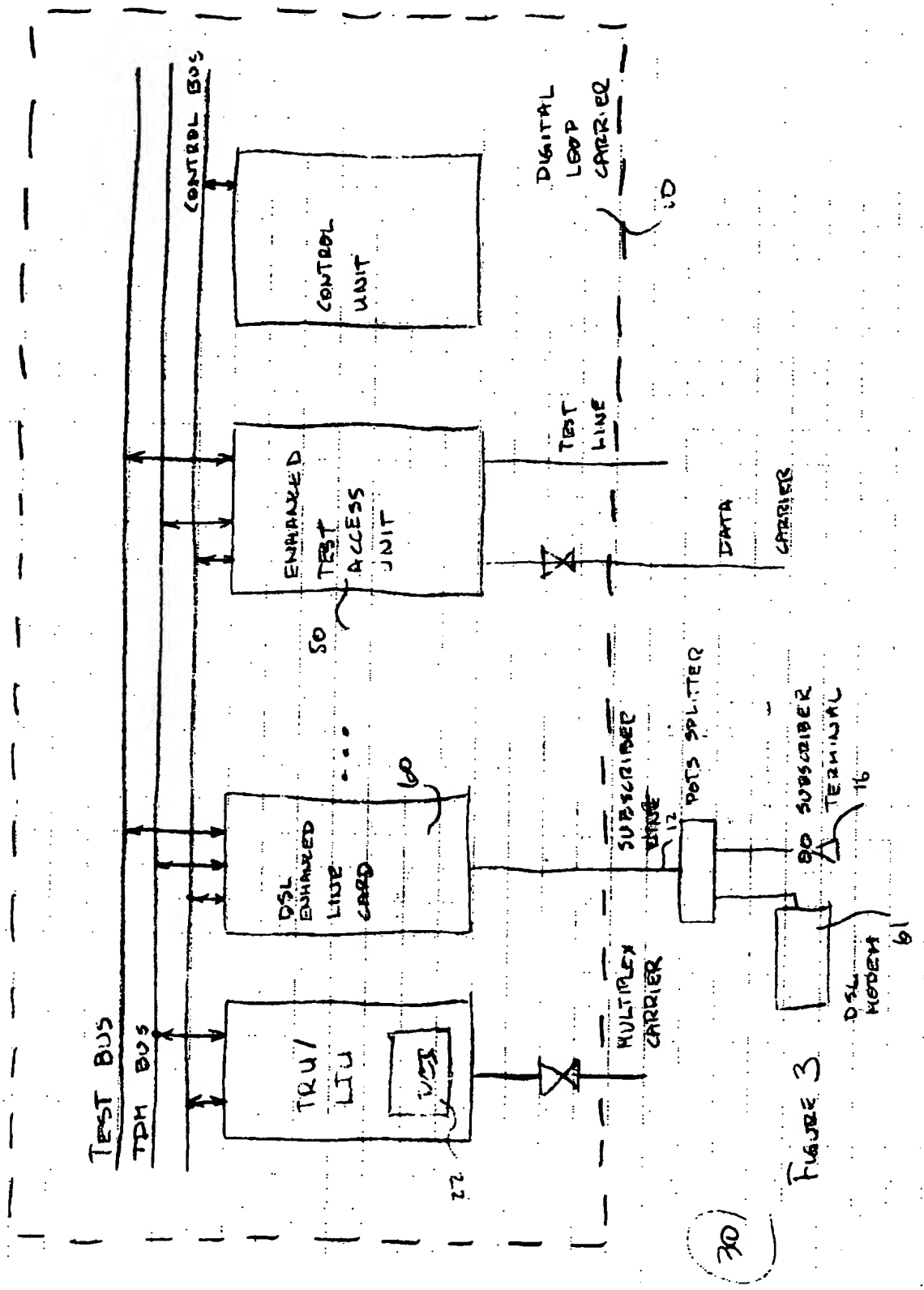
TEST BUS
TDM BUS
CONTROL BUS
TRU/
LTU
DSL
ENHANCED
LINE
CARD
ENHANCED
TEST
ACCESS
UNIT
CONTROL
UNIT
DIGITAL
LOOP
CARRIER
ID
TEST
LINE
DATA
CARRIER
MULTIPLEX
CARRIER
SUBSCRIBER
LINE
POTS SPLITTER
80 SUBSCRIBER
TERMINAL
DSL
MODEM
22
50
60
12
16
61
30

FIGURE 3

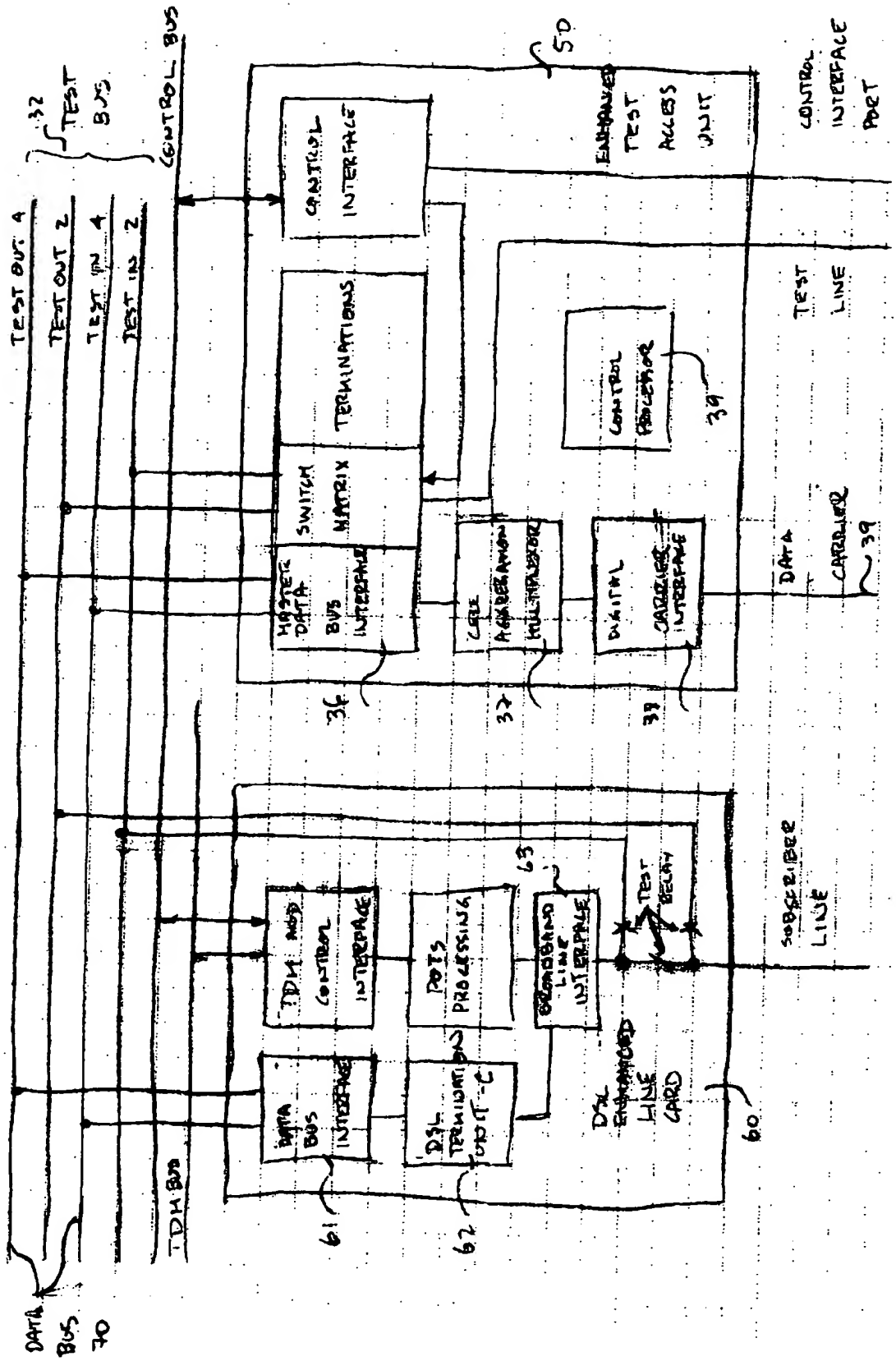
TEST OUT 4
TEST OUT 2
TEST IN 4
TEST IN 2
32
TEST BUS
CONTROL BUS
50
CONTROL INTERFACE
ENHANCED TEST ACCESS UNIT
CONTROL INTERFACE PORT
HOSTED DATA BUS INTERFACE
SWITCH MATRIX
TERMINATIONS
CABLE ASSIGNMENT MULTIPLEXER
DIGITAL CARRIER INTERFACE
CONTROL FUNCTIONS
39
TEST LINE
DATA CARRIER
39
36
32
31
TDM BUS
DATA BUS INTERFACE
TDM BUS CONTROL INTERFACE
POTS PROCESSING
DSL TERMINATION UNIT-C
63
BROADBAND LINE INTERFACE
TEST RELAY
DSL ENHANCED LINE CARD
60
SUBSCRIBER LINE
61
62
DATA BUS
70

FIGURE 4

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